**Amendments to the Claims:**

Claims 1, 10-15, 23, 35, 36 and 52 have been amended herein. Please note that all claims currently pending and under consideration in the referenced application are shown below. Please enter these claims as amended. This listing of claims will replace all prior versions and listings of claims in the application.

**Listing of Claims:**

1. (Currently Amended) A semiconductor die assembly comprising:

a first semiconductor die having an active surface, an opposing back side and a side extending transversely therebetween;

a plurality of bond pads over the active surface in a first arrangement; and

a flexible dielectric interposer substrate having first and second opposing sides and first and second adjacent portions laterally separated by a spacer portion; and

~~and~~the first portion including a first plurality of electrical contacts on the first side ~~of the first portion~~ thereof connected to substantially all of the bond pads of the plurality and communicating through conductive traces with at least a second plurality of electrical contacts on the second side of the second portion in a second arrangement different from the first arrangement ~~on the second side of the second portion~~, said flexible dielectric interposer further including a third plurality of electrical contacts on the second side of the first portion in a third arrangement different from the first arrangement and in communication with at least one of the first plurality of electrical contacts and the second plurality of electrical contacts through conductive traces;

wherein substantially all of the first portion of the interposer substrate extends and is secured over the active surface of the first semiconductor die, substantially all of the second portion is secured over the back side thereof and the spacer portion extends over the side thereof.

2. (Previously presented) The semiconductor die assembly of claim 1, further including discrete conductive elements disposed over the electrical contacts of the second plurality and projecting transversely therefrom.

3. (Original) The semiconductor die assembly of claim 2, wherein the second arrangement comprises a two-dimensional array.

4. (Canceled)

5. (Previously presented) The semiconductor die assembly of claim 1, wherein the third arrangement is a mirror image of the second arrangement.

6. (Original) The semiconductor die assembly of claim 5, wherein the second arrangement comprises a two-dimensional array.

7. (Previously presented) The semiconductor die assembly of claim 1, further including discrete conductive elements disposed over the electrical contacts of the third plurality and projecting transversely to the active surface of the first semiconductor die.

8. (Previously presented) The semiconductor die assembly of claim 1, further including discrete conductive elements disposed over the electrical contacts of one of the second plurality and the third plurality and projecting transversely therefrom.

9. (Previously presented) The semiconductor die assembly of claim 8, further including a second semiconductor die disposed over the first semiconductor die and in electrical communication with the first semiconductor die through another of the second plurality and the third plurality of electrical contacts.

10. (Currently Amended) The semiconductor die assembly of claim 9, wherein the second semiconductor die includes discrete conductive elements projecting transversely therefrom, by which the electrical communication with the first semiconductor die is effected.

11. (Currently Amended) The semiconductor die assembly of claim 10, wherein the second semiconductor die is configured substantially identically to the first semiconductor die.

12. (Currently Amended) The semiconductor die assembly of claim 1, further including an underfill material disposed between the active surface of the first semiconductor die and the first side of the first portion of the interposer substrate.

13. (Currently Amended) The semiconductor die assembly of claim 1, further comprising an adhesive layer over the back side of the first semiconductor die securing the second portion of the interposer substrate thereto.

14. (Currently Amended) The semiconductor die assembly of claim 1, wherein the first and second portions of the interposer substrate are each of a length and width substantially corresponding to a length and width of the first semiconductor die.

15. (Currently Amended) A semiconductor die assembly comprising:

a first semiconductor die having an active surface, an opposing back side, a side extending transversely therebetween and a plurality of bond pads over the active surface in a first arrangement;

a second semiconductor die having an active surface, an opposing back side, a side extending transversely therebetween and a plurality of bond pads over the active surface thereof in a second arrangement; and

a flexible dielectric interposer substrate having first and second opposing sides and first and second adjacent portions laterally separated by a first spacer portion and including:

a first plurality of electrical contacts on the first side of the first portion connected to substantially all of the bond pads of the plurality of the first semiconductor die;

a second plurality of electrical contacts on the second side of the first portion connected to substantially all of the bond pads of the plurality of the second semiconductor die; and

a third plurality of electrical contacts on at least one of the first and second sides of the second portion and in communication through conductive traces with the first and second pluralities of electrical contacts, the third plurality of contacts being in a third arrangement differing from the first and second arrangements;

wherein substantially all of the first portion of the interposer substrate extends and is secured between the first and second semiconductor dice, substantially all of the second portion is secured over the back side of one of the first and second semiconductor dice with the electrical contacts of the third plurality accessible and the first spacer portion extends over the side of the one of the first and second semiconductor dice to which the second portion is secured.

16. (Original) The semiconductor die assembly of claim 15, wherein the first and second arrangements are identical.

17. (Previously presented) The semiconductor die assembly of claim 15, wherein the second arrangement comprises a mirror image of the first arrangement.

18. (Original) The semiconductor die assembly of claim 15, wherein the third plurality of electrical contacts is exposed on both the first and second sides of the second portion.

19. (Previously presented) The semiconductor die assembly of claim 18, wherein the electrical contacts of the third plurality comprise conductive material-filled vias extending from

the first side of the second portion to the second side of the second portion of the interposer substrate.

20. (Previously presented) The semiconductor die assembly of claim 18, further comprising discrete conductive elements disposed on and projecting transversely from accessible electrical contacts of the third plurality.

21. (Previously presented) The semiconductor die assembly of claim 15, further comprising discrete conductive elements disposed on and projecting transversely from accessible electrical contacts of the third plurality.

22. (Previously presented) The semiconductor die assembly of claim 15, wherein the third arrangement comprises a two-dimensional array.

23. (Currently Amended) The semiconductor die assembly of claim 15, wherein the second portion of the interposer substrate comprises two adjacent second portions ~~separated~~ laterally separated by a second spacer portion, substantially all of one second portion is secured over the back side of one of the first and second semiconductor dice, substantially all of the other adjacent second portion is secured over the back side of another of the first and second semiconductor dice, the first spacer portion extends over a side of the one of the first and second semiconductor dice and the second spacer portion extends over ~~the~~ a side of ~~the another~~both of the first and second semiconductor dice.

24. (Previously presented) The semiconductor die assembly of claim 23, wherein the third plurality of electrical contacts is disposed on one of the two adjacent second portions.

25. (Previously presented) The semiconductor die assembly of claim 24, further including discrete conductive elements disposed on the electrical contacts of the third plurality and projecting transversely therefrom.

26. (Previously presented) The semiconductor die assembly of claim 24, further comprising a fourth plurality of electrical contacts disposed on another of the two adjacent second portions and in communication with electrical contacts of at least one of the first and second plurality through conductive traces.

27. (Previously presented) The semiconductor die assembly of claim 26, further including discrete conductive elements disposed on the electrical contacts of either the third plurality or the fourth plurality and projecting transversely therefrom.

28. (Previously presented) The semiconductor die assembly of claim 27, further including at least another semiconductor die disposed over the semiconductor die assembly and in electrical communication with the semiconductor die assembly through electrical contacts of either the third or fourth plurality having no discrete conductive elements disposed thereon.

29. (Original) The semiconductor die assembly of claim 28, wherein the at least another semiconductor die includes discrete conductive elements projecting transversely therefrom, by which the electrical communication with the semiconductor die assembly is effected.

30. (Original) The semiconductor die assembly of claim 29, wherein the at least another semiconductor die assembly comprises another multiple-die assembly.

31. (Original) The semiconductor die assembly of claim 15, further including an underfill material respectively disposed between the active surfaces of the first semiconductor die and the second semiconductor die and the first and second sides of the first portion of the interposer substrate.

32. (Previously presented) The semiconductor die assembly of claim 15, further comprising an adhesive layer over the back side of the one of the first semiconductor die and the second semiconductor die having the second portion of the interposer substrate secured thereto.

33. (Previously presented) The semiconductor die assembly of claim 15, wherein the first and second portions of the interposer substrate are each of a length and width substantially corresponding to a length and width of at least one of the first semiconductor die and the second semiconductor die.

34. (Canceled)

35. (Currently Amended) A semiconductor die assembly comprising:
first and second semiconductor dice having mutually facing active surfaces;
a flexible dielectric interposer substrate having first and second opposing sides and first and second adjacent portions laterally separated by a spacer portion, substantially all of the first portion being disposed between the first and second semiconductor dice and substantially all of the second portion being secured over a back side of one of the first and second semiconductor dice with the spacer portion extending over a side of the semiconductor die over which the second portion is secured, the interposer substrate further including conductive traces electrically respectively electrically connected to substantially all of the first and second semiconductor dice on the first and second opposing sides of the first portion and extending between the first portion and the second portion to an array of discrete conductive elements projecting from the second portion on the back side of the one of the first and second semiconductor dice to which the second portion is secured.

36. (Currently Amended) An interposer substrate for use with at least one semiconductor die having an active surface and a back side, the interposer substrate comprising:

a flexible dielectric substrate having a first portion sized and configured to correspond to an active surface of a first selected semiconductor die and an adjacent second portion laterally separated by a spacer portion and sized and configured to correspond to an active surface of a second selected semiconductor die;

a first plurality of electrical contacts on a first side of the first portion arranged to mate with substantially of the bond pads of ~~a~~ the first selected semiconductor die and connected to a second plurality of electrical contacts on a side of a second portion of the interposer substrate through conductive traces, the second plurality of electrical contacts being in a different arrangement than the first plurality of electrical contacts; and

a third plurality of electrical contacts on a second side of the first portion, arranged to mate with substantially all of the bond pads of ~~a~~ the second selected semiconductor die and electrically connected through conductive traces to electrical contacts of the second plurality.

37. (Canceled)

38. (Previously presented) The interposer substrate of claim 36, further comprising a fourth plurality of electrical contacts on another side of the second portion electrically connected to the electrical contacts of the first and third pluralities through conductive traces.

39. (Original) The interposer substrate of claim 38, wherein the second and fourth pluralities of electrical contacts are connected.

40. (Previously presented) The interposer substrate of claim 39, wherein the second and fourth pluralities of electrical contacts lie at opposing ends of conductive vias extending transversely through the second portion.

41. (Previously presented) The interposer substrate of claim 38, wherein the second and fourth pluralities of electrical contacts comprise two-dimensional arrays.

42. (Original) The interposer substrate of claim 41 wherein the two-dimensional arrays comprise mirror images.

43-51. (Canceled)

52. (Currently Amended) An electronic assembly, comprising:

a semiconductor die assembly comprising:

first and second semiconductor dice having mutually facing active surfaces;

a flexible dielectric interposer substrate having first and second opposing sides and first and second adjacent portions laterally separated by a spacer portion, substantially all of the first portion being disposed between the first and second semiconductor dice and substantially all of the second portion being secured over a back side of one of the first and second semiconductor dice with the spacer portion extending over a side of the semiconductor die over which the second portion is secured, the interposer substrate further including conductive traces respectively electrically connected to substantially all of the bond pads of the first and second semiconductor dice on opposing sides of the first portion and extending between the first portion and the second portion to an array of discrete conductive elements projecting from the second portion on the back side of the one of the first and second semiconductor dice to which the second portion is secured; and

a higher level packaging structure connected to the semiconductor die assembly through the discrete conductive elements.

53. (Original) The electronic assembly of claim 52, wherein the higher level packaging structure comprises a computer.